REMARKS

Applicants respectfully request that the Amendment and Response to Final Office Action be admitted under 37 C.F.R. 1.116. Applicants submit that this amendment presents claims in better form for consideration on appeal. Furthermore, applicants believe that consideration of this amendment could lead to favorable action that would remove one or more issues for appeal. Applicants submit that thus there is good and sufficient reason why this amendment should be admitted now. Reconsideration of this application, as amended, is respectfully requested.

Claims 63-90 are pending. Claims 63-90 stand rejected.

Claims 63 and 76 have been amended. Claims 77-90 have been cancelled. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicants submit that the amendments do not add new matter.

Rejections Under 35 U.S.C. § 102(e)

Claims 63-75 and 77-89 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,063,681 of Son ("Son"). The Examiner stated that

> With regard to Claim 63, Son teaches a substrate (21), a gate electrode (25) formed over the substrate and defining an underlying channel region in the substrate, said gate electrode having a barrier layer (26) formed on a sidewall of the gate electrode to prohibit silicidation of the sidewall, a source/drain extension (27) formed in the substrate adjacent the gate electrode and having a first silicide layer (29) formed therein, and a source/drain (30) formed in the substrate adjacent the source/drain extension and having an activated doped region with a second silicide layer (33) disposed therein and wherein the activated doped region and the first silicide are aligned with a spacer (31) disposed along sidewalls of the gate electrode, said source/drain extension (27) having less dopant concentration (LDD) than the activated doped region and the source/drain extension and the first silicide layer (29) are aligned with the gate electrode to have the less dopant concentration of the extension reside between the channel region and the activated doped region. See figure 3H.
>
> The claim also includes the limitation "*said second silicide layer formed after removing a portion of said barrier layer formed over a top surface of the gate electrode*", this is a product by process limitation. A "product by process" claim is directed to the product per se, no matter how actually made, In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re

Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Marosi et al, 218 USPQ 289; and particularly In re Thorpe, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear.

(Office Action mailed March 19, 2003, page 2, paragraph 3 – page 4, paragraph 1)

Son discloses that

Referring to FIG. 3A, the method for fabricating a semiconductor device in accordance with a first preferred embodiment of the present invention starts with forming trenches (not shown) in field regions of an N type semiconductor substrate 21 having an active region and the field regions defined therein. A first oxide film is deposited on the semiconductor substrate 21 to cover the trenches and subjected to chemical mechanical polishing to make the first oxide film flat to the semiconductor substrate 21, to form isolating insulating films 22. P type boron ions injected into the active region to form a P well 23 therein. Then, ions are injected into the active region in the P well 23 for adjusting a channel threshold voltage. A second oxide film and a doped silicon layer are deposited on the semiconductor substrate 21 in succession and etched anisotropicially using a mask to form a gate, to form a gate oxide film 24 and a gate electrode 25. The first silicon layer may be doped as it is deposited, or after completion of the deposition by injecting ions. As shown in FIG. 3B, after subjecting the semiconductor substrate 21 to thermal oxidation to form a thin film on an entire surface of the semiconductor substrate 21 or after depositing a thin third oxide film or a nitride film, the film is subjected to anisotropic etching, to form first sidewall spacers 26 at both sides of the gate oxide film 24 and the gate electrode 25 to a thickness ranging 100-500A. As shown in FIG. 3C, the semiconductor substrate 21 on both dies of the gate electrode 25 and the first sidewall spacers 26 is lightly doped with N type impurity ions to form LDD regions 27 therein. As shown in FIG. 3D, a first metal layer 28 is deposited on an entire surface of the semiconductor substrate 21 to a thickness ranging 100-200 A. As shown in FIG. 3E, the first metal layer 28 formed on the entire surface is annealed to form a first metal silicide 29 on top of the gate electrode 25 and in surfaces of the LDD regions 27. Then, the metal layer 28 which made no reaction is removed. N type impurity ions are injected heavily to form source/drain regions 30. As shown in FIG. 3F, an oxide film is deposited and etched back, to form second sidewall spacers 31 on both sides of the first sidewall spacers 26. As shown in FIG. 3G, a thick second metal layer 32 is deposited on an entire surface of the semiconductor substrate 21. The metal layer 32 may be formed thin with a thickness ranging 100-300A. The first, and second metal layer 28 and 32 may be formed of titanium, nickel, or cobalt. As shown in FIG. 3H, a second metal silicide 33 is formed at a portion in contact with the first metal silicide 29 by thermal process. The source/drain regions 30 are activated by annealing thereafter.

(Son Col. 3, line 30 – Col. 4, line 9)

Applicants respectfully submit that claims 63-75 and 77-89 are not anticipated by Son under 35 U.S.C. 102 § (e). Amended claim 63 includes the following limitations.

> A microelectronic structure comprising:
> a substrate;
> a gate electrode formed over the substrate and defining an underlying channel region in the substrate, said gate electrode having a barrier layer formed on a sidewall of the gate electrode to prohibit the silicidation of the sidewall;
> a source/drain extension formed in the substrate adjacent the gate electrode and encroaching laterally into the underlying channel region a first distance, the source/drain extension having a first silicide layer formed therein, the first silicide encroaching laterally into the underlying channel region a second distance less than the first distance; and
> a source/drain region formed in the substrate adjacent the source/drain extension and having an activated doped region with a second silicide layer disposed therein, the activated doped region and the second silicide layer are aligned with a spacer disposed along sidewalls of the gate electrode such that <u>the activated doped region and the second silicide layer encroach laterally into the underlying channel region a third distance less than the second distance</u>, said source/drain extension having less dopant concentration than the activated doped region.

(Amended claim 63) (Emphasis added)

It is clear from the way in which the semiconductor device of Son is fabricated that the source/drain region 30 extends into the channel region at least as far as the first sidewall spacer 26. That is, since the ion implantation takes place after the formation of the first sidewall spacer 26, but prior to the formation of the second sidewall spacer 31, the source/drain region 30 would extend at least as far as sidewall space 26. Figures 3E – 3H of Son show the source/drain region 30 extending not as far as first sidewall 26 and thus the figures are misleading. However, the figures show the source/drain region 30 extending beyond the second sidewall spacer 31 (see Figures 2 and 3H). Also note that Figures 2 and 3H show, correctly, that the second silicide layer 33 would extend no further than the second sidewall spacer 31.

In contrast, the source/drain region of the claimed present invention, for example as claimed in amended claim 63 extends into the channel region only as far as the second silicide

layer. Moreover, both the channel region and the second silicide layer are aligned with the gate electrode sidewall (equated by the examiner with the second sidewall spacer 31 of Son).

Applicants, therefore respectfully submit that amended claim 63 is not anticipated by Son. Given that claims 64-76 depend, directly of indirectly from claim 63, applicants respectfully submit that claims 64-76 are likewise not anticipated by Son.

Rejections Under 35 U.S.C. § 103(a)

Claims 76 and 90 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Son. The Examiner has stated that

> With regard to Claims 76 and 90, Son essentially teaches the claimed invention but fails to show, the source/drain extension having a thickness 300-500 angstroms in thickness. It would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Son to include an extension having a thickness 300-500 angstroms in thickness, in order to control short channel effect and therefore increase the speed of the transistor. Additionally, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

(Office Action mailed March 19, 2003, page 7, paragraph 6)

Applicants respectfully submit that amended claim 76 is not obvious under 35 U.S.C. § 103(a) in view of Son. Amended claim 76 includes the following limitation.

> The microelectronic structure of claim 63, wherein the source/drain extension is <u>more than 400</u> angstroms in thickness.

(Amended claim 76) (Emphasis added).

Son teaches away from a source/drain extension in excess of 400 angstroms. For example, Son explicitly states that the "first metal silicide" is formed to a depth of 200 – 400 angstroms. Son also teaches that the "second metal silicide" is deeper than the first metal silicide and may be 500 angstroms, thus precluding 500 angstroms as a depth for the first metal silicide.

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome. If there are any additional charges, please charge Deposit Account No. 02-2666 for any fee deficiency that may be due.

Respectfully submitted,

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Date: 6/24/03

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